ML610Q346/ML610346

8-bit Microcontroller with Voice Output Function

GENERAL DESCRIPTION

Equipped with an LAPIS Semiconductor original 8-bit CPU nX-U8/100, the ML610Q346/ML610346 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as an op-amp, 12-bit A/D converter, timer, synchronous serial port, UART, and voice output function. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture. The microcontroller is also equipped with a flash memory that has achieved low voltage and low power consumption (at read) equivalent to mask ROMs, so it is best suited to battery-driven applications such as cellular phones. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction repertoire: 16-bit length instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logical operations, multiply/divide operations, bit manipulation, bit logical operations, jump, conditional jump, call return stack manipulation, and arithmetic shift instructions.
  - Built-in on-chip debugging function
  - Minimum instruction execution time:
    31.25 µs (@ 32kHz system clock)
    0.244 µs (@ 4.096 MHz system clock)

- Internal memory
  - ML610Q346
    Has 128-Kbyte flash memory (64K × 16-bit) built in. (including unusable 1KByte TEST area)
  - ML610346
    Has 128-Kbyte mask memory (64K × 16-bit) built in. (including unusable 1KByte TEST area)
  - Has 1-Kbyte RAM (1024 × 8-bit) built in.

- Interrupt controller
  - Non-maskable interrupt: 2 sources (1 internal source and 1 external sources)
  - Maskable interrupt: 18 sources (10 internal sources and 8 external sources)

- Time-base counter
  - Low-speed side time-base counter × 1ch
  - High-speed side time-base counter × 1ch

- Watchdog timer
  - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  - Free-running
  - Selectable overflow period: 4 types (125 ms, 500 ms, 2 sec, 8 sec)

- Timer
  - 8-bit × 2ch (16-bit configuration also enabled)

- Voice output function
  - Voice synthesis method: HQ-ADPCM / 4-bit ADPCM2 / 8-bit non-linear PCM / 8-bit PCM / 16-bit PCM
  - Sampling frequency: 6.4/8/10.7/12.8/16/21.3/25.6/32 kHz

- Speaker amplifier output power
  - 1W(at 5V)

- Synchronous serial port
  - Master/slave selectable
  - LSB/MSB-first selectable
  - 8-bit/16-bit length selectable

- UART
  - Half-Duplex Communication
  - TXD/RXD × 1 channel
  - Bit length, with/without parity, odd/even parity, 1 or 2 stop bits
  - Positive/negative logic selectable
  - Built-in baud-rate generator

- Successive-approximation type A/D converter
  - 12-bit A/D converter
  - Input: 3ch
  - Conversion time: 26.86 µs per channel at 4.096 MHz

- Op-amp
  - 3ch
  - Composition is possible as reversal amplifier, reversed amplifier, and a comparator.

- General-purpose port
  - Input-only port × 8ch
  - Output-only port × 4ch (those as secondary functions are also included)
  - Input-output port × 16ch (those as secondary functions are also included)

- Reset
  - Resetting by the RESET_N pin
  - Resetting upon power-on detection
  - Resetting upon WDT overflow detection

- Clock
  - Low-speed side clock
    Built-in RC oscillator (32 kHz)
  - High-speed side clock
    Crystal/ceramic oscillation (4.096 MHz), external clock

- Power management
  - HALT mode: Halts the execution of instructions issued by the CPU (the peripheral circuits continue operating)
  - STOP mode: Stops low-speed and high-speed oscillation (the CPU and the peripheral circuits stop operating)
  - Clock gear: Allows changing the frequency of the high-speed system clock by software (oscillator clock divided by 1, 2, 4, or 8)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - 64-pin TQFP
  - High-speed side clock : Crystal/ceramic oscillation (4.096 MHz)
    Flash Memory : ML610Q346-xxxTB (blank product: ML610Q346-NNNTB)
    Mask Memory : ML610346-xxxTB

  - High-speed side clock : external clock
    Flash Memory : ML610Q346J-xxxTB (blank product: ML610Q346J-NNNTB)
    Mask Memory : ML610346J-xxxTB

    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: −40°C to +85°C
  - Operating voltage: V_{DD} = 2.2 to 5.5 V, SPV_{DD} = 2.3 to 5.5 V, AV_{DD} = 2.2 to 5.5 V
    (Be sure to apply the same voltage to V_{DD} and SPV_{DD} power supplies.)

BLOCK DIAGRAM

Figure 1 is a block diagram of the ML610Q346.
Symbols with an asterisk "*" indicate that each of them is the secondary or tertiary function of the corresponding port.

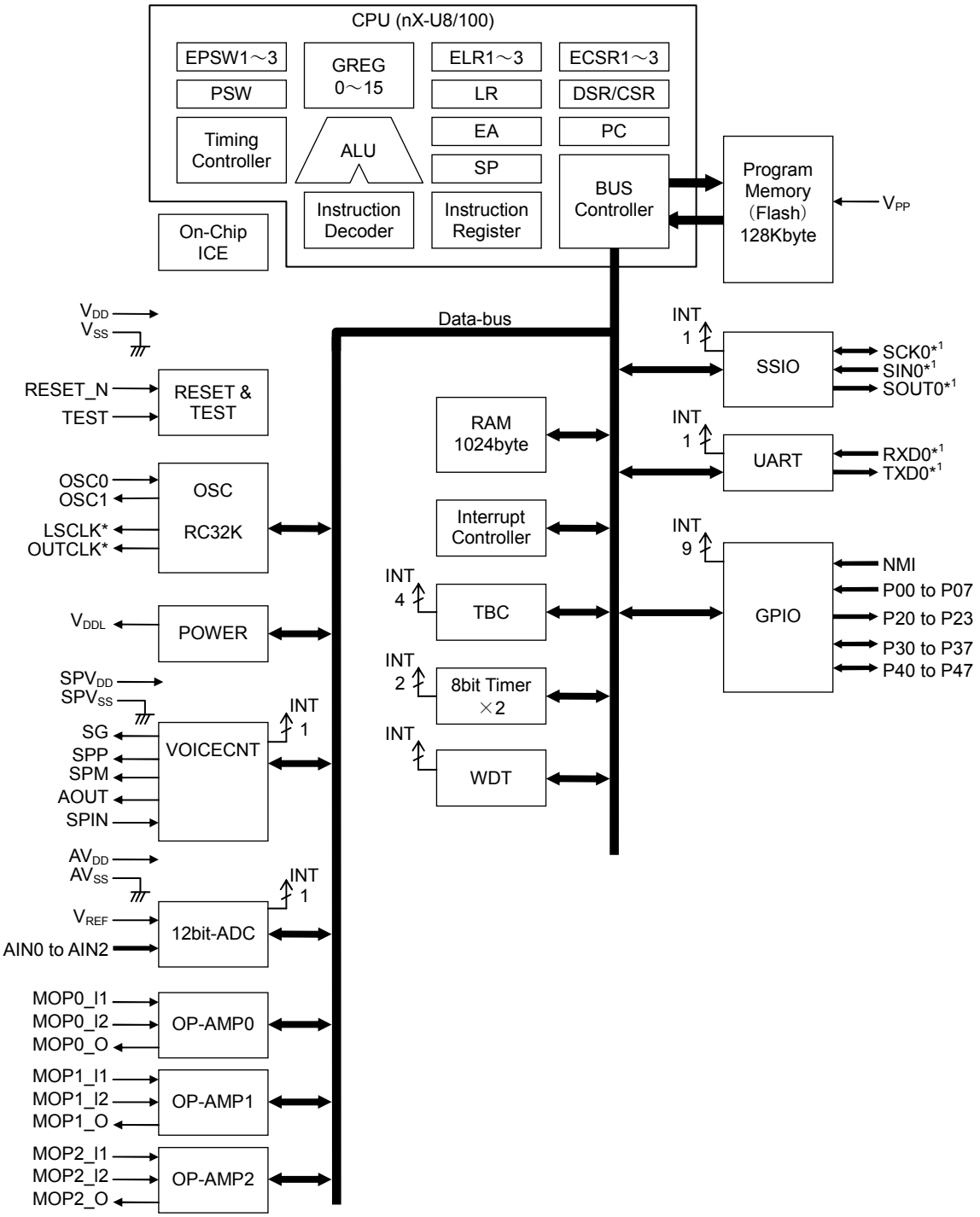


Figure 1 Block Diagram of ML610Q346

Figure 2 is a block diagram of the ML610346.
Symbols with an asterisk "*" indicate that each of them is the secondary or tertiary function of the corresponding port.

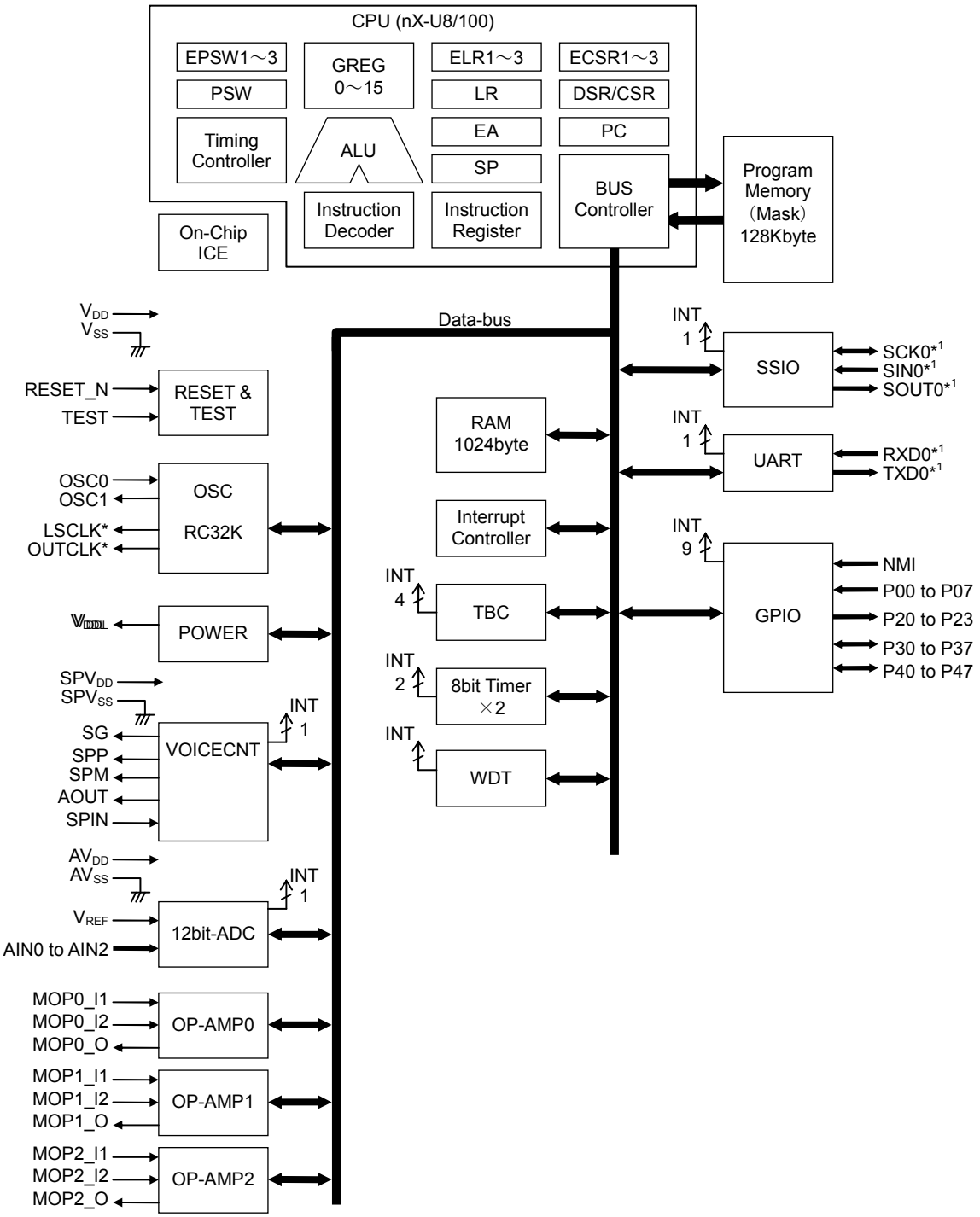
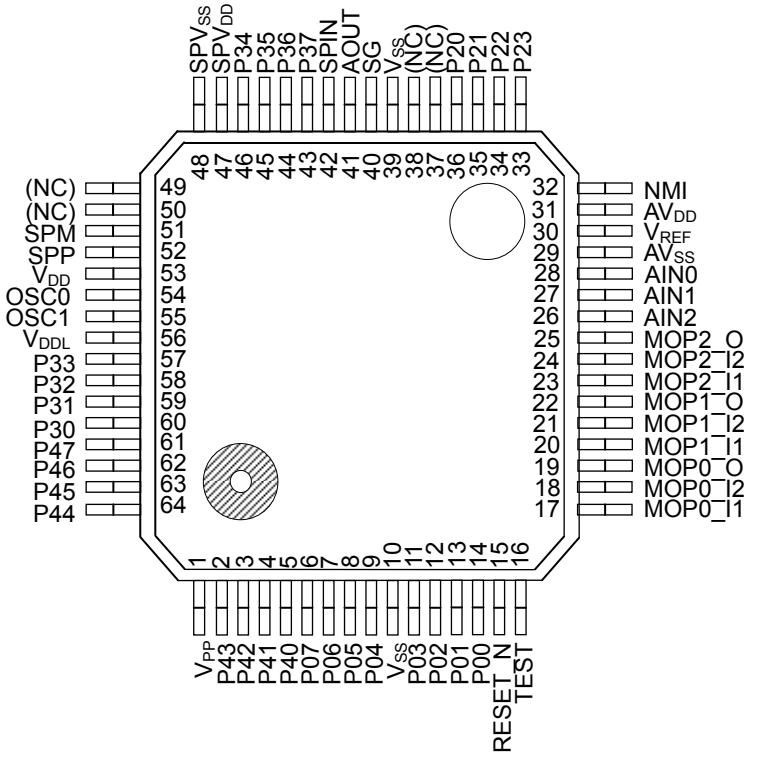


Figure 2 Block Diagram of ML610346

PIN CONFIGURATION

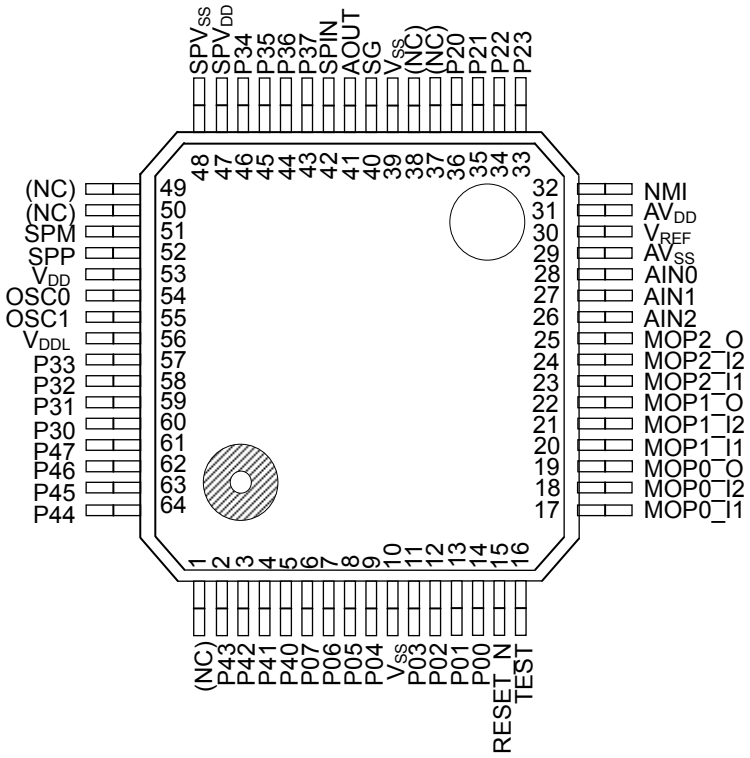
ML610Q346 TQFP package product



NC: No Connection

Figure 3 Pin Configuration of ML610Q346 Package Product

ML610346 TQFP package product



NC: No Connection

Figure 4 Pin Configuration of ML610346 Package Product

LIST OF PINS

PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
10,39	Vss	—	Negative power supply pin	—	—	—	—	—	—
53	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
56	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—
48	SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—	—	—	—	—
47	SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—	—	—	—	—
29	AV_{SS}	—	Negative power supply pin for successive-approximation type ADC/OP-amp	—	—	—	—	—	—
31	AV_{DD}	—	Positive power supply pin for successive-approximation type ADC/OP-amp	—	—	—	—	—	—
1	V_{PP}(*)	—	Power supply pin for flash memory	—	—	—	—	—	—
16	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
15	RESET_N	I	Reset input pin	—	—	—	—	—	—
54	OSC0	I	Connection pin for high-speed clock oscillation	—	—	—	—	—	—
55	OSC1	O	Connection pin for high-speed clock oscillation	P11	I	Input port	—	—	—
41	AOUT	O	LINE output	—	—	—	—	—	—
42	SPIN	I	Analog input to the built-in speaker amplifier	—	—	—	—	—	—
40	SG	O	Reference power supply pin of the built-in speaker amplifier	—	—	—	—	—	—
52	SPP	O	Positive output pin of the built-in speaker amplifier	—	—	—	—	—	—
51	SPM	O	Negative output pin of the built-in speaker amplifier	—	—	—	—	—	—
30	V_{REF}	—	Reference power supply pin for successive-approximation type ADC	—	—	—	—	—	—
28	AIN0	I	Successive-approximation type ADC input	—	—	—	—	—	—
27	AIN1	I	Successive-approximation type ADC input	—	—	—	—	—	—
26	AIN2	I	Successive-approximation type ADC input	—	—	—	—	—	—

PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
32	NMI	I	Input port, non-maskable interrupt	—	—	—	—	—	—
14	P00/EXI0	I	Input port / External interrupt	—	—	—	—	—	—
13	P01/EXI1	I	Input port / External interrupt	—	—	—	—	—	—
12	P02/EXI2/ RXD0	I	Input port / External interrupt / UART0 data input	—	—	—	—	—	—
11	P03/EXI3	I	Input port / External interrupt	—	—	—	—	—	—
9	P04/EXI4/ T0P0CK	I	Input port / External interrupt / Timer 0 external clock input	—	—	—	—	—	—
8	P05/EXI5/ T1P1CK	I	Input port / External interrupt / Timer 1 external clock input	—	—	—	—	—	—
7	P06/EXI6	I	Input port / External interrupt	—	—	—	—	—	—
6	P07/EXI7	I	Input port / External interrupt	—	—	—	—	—	—
36	P20/LED0	O	Output port / LED drive	LSCLK	O	Low-speed clock output	—	—	—
35	P21/LED1	O	Output port / LED drive	OUTCLK	O	high-speed clock output	—	—	—
34	P22/LED2	O	Output port / LED drive	—	—	—	—	—	—
33	P23/LED3	O	Output port / LED drive	—	—	—	—	—	—
60	P30	I/O	Input/output port	—	—	—	—	—	—
59	P31	I/O	Input/output port	—	—	—	—	—	—
58	P32	I/O	Input/output port	—	—	—	—	—	—
57	P33	I/O	Input/output port	—	—	—	—	—	—
46	P34	I/O	Input/output port	—	—	—	—	—	—
45	P35	I/O	Input/output port	—	—	—	—	—	—
44	P36	I/O	Input/output port	LSCLK	O	Low-speed clock output	—	—	—
43	P37	I/O	Input/output port	OUTCLK	O	high-speed clock output	—	—	—
5	P40	I/O	Input/output port	—	—	—	SIN0	I	SSIO0 data input
4	P41	I/O	Input/output port	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output
3	P42	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output
2	P43	I/O	Input/output port	TXD0	O	UART0 data output	—	—	—
64	P44/T0P0 CK	I/O	Input/output port, Timer 0 external clock input	—	—	—	SIN0	I	SSIO0 data input
63	P45/T1P1 CK	I/O	Input/output port, Timer 1 external clock input	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output
62	P46	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output
61	P47	I/O	Input/output port	—	—	—	—	—	—

PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
17	MOP0_I1	I	Op-amp0 positive analog input	—	—	—	—	—	—
18	MOP0_I2	I	Op-amp0 negative analog input	—	—	—	—	—	—
19	MOP0_O	O	Op-amp0 analog output	—	—	—	—	—	—
20	MOP1_I1	I	Op-amp1 positive analog input	—	—	—	—	—	—
21	MOP1_I2	I	Op-amp1 negative analog input	—	—	—	—	—	—
22	MOP1_O	O	Op-amp1 analog output	—	—	—	—	—	—
23	MOP2_I1	I	Op-amp2 positive analog input	—	—	—	—	—	—
24	MOP2_I2	I	Op-amp2 negative analog input	—	—	—	—	—	—
25	MOP2_O	O	Op-amp2 analog output	—	—	—	—	—	—

*: Applies to the ML610Q346.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated) Capacitors C_L(see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—
SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—
AV_{SS}	—	Negative power supply pin for successive-approximation type ADC/OP-amp	—	—
AV_{DD}	—	Positive power supply pin for successive-approximation type ADC/Op-amp	—	—
V_{PP}(*)	—	Power supply pin for flash memory	—	—
Test				
TEST	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a "H" level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
OSC0	I	Pins for connecting a crystal unit for high speed clock. Connect a 4.096 MHz crystal unit (see Measuring Circuit 1) to these pins. Also, connect capacitors (C_{DH} and C_{GH}) between these pins and V_{SS} as required.	—	—
OSC1	O		—	—
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20 and P36 pins.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 and P37 pins.	Secondary	—
General-purpose Input port				
P00–P07	I	General-purpose input ports.	Primary	Positive
General-purpose Output port				
P20–P23	O	General-purpose output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
General-purpose Input/output port				
P30–P37	I/O	General-purpose input/output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
P40–P47	I/O			

*Applies to the ML610Q346.

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART0 data input pin. Allocated to the primary function of the P02 pin and the secondary function of the P42 pin.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin and P44 pins.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 and P45 pins.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 and P46 pins.	Tertiary	Positive
External interrupt				
NMI	I	External non-maskable interrupt input pin. The interrupt occurs on both the rising and falling edges.	Primary	Positive/ Negative
EXI0–7	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P00–P07 pins.	Primary	Positive/ Negative
Timer				
T0P0CK	I	External clock input pin for timer 0. Allocated to the primary function of the P04 and P44 pins.	Primary	—
T1P1CK	I	External clock input pin for timer 1. Allocated to the primary function of the P05 and P45 pins.	Primary	—
LED drive				
LED0–3	O	NMOS open drain pins to allow direct driving of LED. Allocated to the secondary function of the P20–P22 pins.	Primary	Positive/ Negative
Voice output function				
AOUT	O	LINE output pin. When you use built-in speaker amplifier, connect with the SPIN pin.	—	—
SPIN	I	Analog input pin of the internal speaker amplifier.	—	—
SG	O	Reference voltage output pin of the internal speaker amplifier.	—	—
SPP	O	Positive output pin of the internal speaker amplifier.	—	—
SPM	O	Negative output pin of the internal speaker amplifier.	—	—
Successive-approximation type A/D converter				
V_{REF}	—	Reference power supply pin for the successive-approximation type A/D converter.	—	—
AIN0–AIN2	I	Analog inputs to Ch0 to Ch2 of the successive-approximation type A/D converter.	—	—
Op-amp				
MOP0_I1	I	Positive analog input pins of the op-amp0.	—	—
MOP0_I2	I	Negative analog input pins of the op-amp0.	—	—
MOP0_O	O	Analog output pins of the op-amp0.	—	—
MOP1_I1	I	Positive analog input pins of the op-amp1.	—	—
MOP1_I2	I	Negative analog input pins of the op-amp1.	—	—
MOP1_O	O	Analog output pins of the op-amp1.	—	—
MOP2_I1	I	Positive analog input pins of the op-amp2.	—	—
MOP2_I2	I	Negative analog input pins of the op-amp2.	—	—
MOP2_O	O	Analog output pins of the op-amp2.	—	—

TERMINATION OF UNUSED PINS

How to Terminate Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
RESET_N	Open
TEST	Open
AV_{DD}	V_{SS}
AV_{SS}	V_{SS}
V_{REF}	V_{SS}
AIN0 – AIN2	Open
SPV_{DD}	V_{SS}
SPV_{SS}	V_{SS}
AOUT	Open
SPIN	Open
SG	Open
SPP	Open
SPM	Open
P00–P07	V_{DD} or V_{SS}
P20–P23	Open
P30–P37	Open
P40–P47	Open
MOP0_I1	Open
MOP0_I2	Open
MOP0_O	Open
MOP1_I1	Open
MOP1_I2	Open
MOP1_O	Open
MOP2_I1	Open
MOP2_I2	Open
MOP2_O	Open

Note:
It is recommended to configure the unused input ports and input/output ports as inputs with pull-down resistors/pull-up resistors or outputs since the supply current may become excessively large if those pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = AV_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Power supply voltage 2	AV_{DD}	Ta = 25°C	–0.3 to +7.0	V
Power supply voltage 3	SPV_{DD}	Ta = 25°C	–0.3 to +7.0	V
Power supply voltage 4	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 5	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	P03, P04, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	P02, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	861	mW
Storage temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions

(V_{SS} = AV_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–40 to +85	°C
Operating voltage	V_{DD}	—	2.2 to 5.5	V
	SPV_{DD}	—	2.3 to 5.5	
	AV_{DD}	—	2.2 to 5.5	
Operating frequency (CPU)	f_{OP}	—	27k to 4.2M	Hz
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	4.0M, 4.096M	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	15 to 32	pF
	C_{GH}	—	15 to 32	
Capacitor externally connected to V_{DDL} pin	C_L	—	10±30%	µF
Capacitor externally connected to SG pin	C_{SG}	—	0.1±30%	µF

Flash Memory Operating Conditions

(V_{SS} = AV_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase (*1)	2.7 to 3.6	V
	V_{DDL}	At write/erase (*1)	2.5 to 2.75	
	V_{PP}	At write/erase (*1)	7.7 to 8.3	
Maximum rewrite count	C_{EP}	—	80	times
Data retention period	Y_{DR}	—	10	years

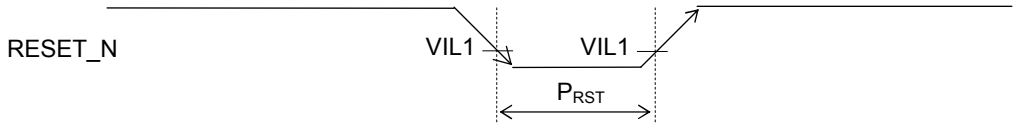
*1: When writing data to, or erasing data from, flash ROM, it is necessary to apply a voltage within the range specified above to the V_{DDL} pin.

DC Characteristics (1 of 5)

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = AV_{SS} = SPV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
High-speed oscillation start time	T_{XTH}	—	—	2	20	ms	1
Low-speed RC oscillator frequency	f_{LCR}	—	27.2k	32k	36.8k	Hz	
Reset pulse width	P_{RST}	—	100	—	—	µs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.4		
Time from power-on reset to power-up	T_{POR}	—	—	—	10	ms	

Reset



Reset by RESET_N pin

Power-on reset

DC Characteristics (2 of 5)

(V_{DD} = SPV_{DD} = 2.3 to 5.5V, AV_{DD} = 2.2 to 5.5V, V_{SS} = AV_{SS} = SPV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
LINE amplifier output load resistance	R_{LA}	At 1/2V_{DD} output	10	—	—	kΩ	
LINE amplifier output voltage range	V_{AD}	At output load	DV_{DD}×1/6	—	DV_{DD}×5/6	V	
SG output voltage	V_{SG}	—	0.95 × DV_{DD}/2	DV_{DD}/2	1.05 × DV_{DD}/2	V	
SG output resistance	R_{SG}	—	57	96	135	kΩ	
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω	
Speaker amplifier output power	PSPO1	SPV_{DD} = 3.3V, f = 1kHz, RSPO = 8Ω, THD ≥ 10% At SPIN Input	—	0.5	—	W	1
	PSPO2	SPV_{DD} = 5.0V, f = 1kHz, RSPO = 8Ω, THD ≥ 10% At SPIN Input	—	1	—	W	
Output offset voltage between SPM and SPP with no signal present	VOF	SPV_{DD}=3.0V, SPIN – SPM gain = +6dB With a load of 8Ω	–50	—	+50	mV	

Electrical Characteristics of Op-Amp

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DDOP}	VDD = 3.0V, one op-amp used	—	50	80	μA
		VDD = 5.0V, one op-amp used	—	60	90	μA
Input voltage range	V_{IP}	—	V_{SS} –0.1	—	AV_{DD} –1.2	V
High-level output voltage	V_{OH}	If = –150μA	AV_{DD} –0.1	—	AV_{DD}	V
Low-level output voltage	V_{OL}	If = –150μA	V_{SS}	—	V_{SS} +0.1	V
Input offset	V_{IO}	—	–10	—	+10	mV
Output current	I_{OUT}	When configured as a non-inverting op-amp (Gain = 1) VDD = 3.0V, Vout = 0.5 to 1.8V	—	—	1	mA

DC Characteristics (3 of 5) ML610Q346

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = AV_{SS} = SPV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped	Ta ≤ +40°C	—	0.5	2.0	μA	1
			Ta ≤ +85°C	—	0.5	8		
Supply current 2	IDD2	CPU: In HALT state (LTBC: Operating*3) High-speed oscillation:Stopped	Ta ≤ +40°C	—	1.5	3.0		
			Ta ≤ +85°C	—	1.5	10		
Supply current 3	IDD3	CPU: Running at 32 kHz*1 High-speed oscillation: Stopped		—	10	35		
Supply current 4	IDD4	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode*2	V_{DD} = AV_{DD} = SPV_{DD} = 3.0V	—	1.7	4	mA	
			V_{DD} = AV_{DD} = SPV_{DD} = 5.0V	—	2.2	4		
Supply current 5	IDD5	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode*2 During voice playback (no output load)	V_{DD} = AV_{DD} = SPV_{DD} = 3.0V	—	3	12		
			V_{DD} = AV_{DD} = SPV_{DD} = 5.0V	—	8	12		
Supply current 6	IDD6	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode*2 ADC: Operating	V_{DD} = AV_{DD} = SPV_{DD} = 3.0V	—	1.9	5.5		
			V_{DD} = AV_{DD} = SPV_{DD} = 5.0V	—	3.2	5.5		

*1: Case when the CPU operating rate is 100% (with no HALT state)
*2 : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).
*3 : Significant bits of BLKCON0~BLKCON4 registers are all “1”.

DC Characteristics (3 of 5) ML610346

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = AV_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped	Ta ≤ +40°C	—	0.5	2.0	μA	1
			Ta ≤ +85°C	—	0.5	8		
Supply current 2	IDD2	CPU: In HALT state (LTBC: Operating*3) High-speed oscillation:Stopped	Ta ≤ +40°C	—	1.2	3.0		
			Ta ≤ +85°C	—	1.2	10		
Supply current 3	IDD3	CPU: Running at 32 kHz*1 High-speed oscillation: Stopped		—	5	35		
Supply current 4	IDD4	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode*2	V_{DD} = AV_{DD} = SPV_{DD} = 3.0V	—	1	4	mA	
			V_{DD} = AV_{DD} = SPV_{DD} = 5.0V	—	2	4		
Supply current 5	IDD5	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode*2 During voice playback (no output load)	V_{DD} = AV_{DD} = SPV_{DD} = 3.0V	—	2.8	12		
			V_{DD} = AV_{DD} = SPV_{DD} = 5.0V	—	8	12		
Supply current 6	IDD6	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode*2 ADC: Operating	V_{DD} = AV_{DD} = SPV_{DD} = 3.0V	—	1.1	5.5		
			V_{DD} = AV_{DD} = SPV_{DD} = 5.0V	—	2.3	5.5		

*1: Case when the CPU operating rate is 100% (with no HALT state)
*2 : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).
*3 : Significant bits of BLKCON0~BLKCON4 registers are all “1”.

DC Characteristics (4 of 5)

(V_{DD} = SPV_{DD} = APV_{DD} = 2.2 to 5.5V, V_{SS} = AV_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

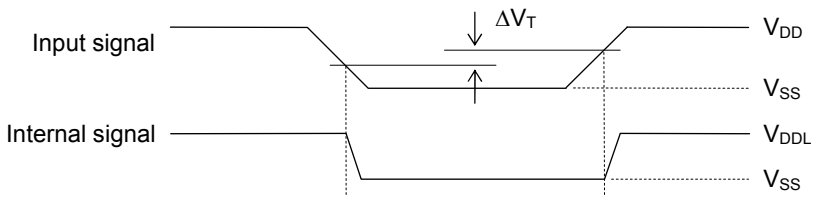
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20–P23) (P30–P37) (P40–P47)	VOH1	IOH1 = –0.5mA		V_{DD} –0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20–P23)	VOL2	When LED drive mode is selected	IOL2 = +5mA $V_{DD} \geq 2.2V$	—	—	0.5		
			IOL2 = +8mA $V_{DD} \geq 2.3V$	—	—	0.5		
Output leakage current (P20–P23) (P30–P37) (P40–P47)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	–1	µA	4
	IIL1	VIL1 = V_{SS}		–1500	–300	–20		
Input current 2 (NMI) (P00–P07) (P11) (P30–P37) (P40–P47)	IIH2	VIH2 = V_{DD} (when pulled down)		2	30	250		
	IIL2	VIL2 = V_{SS} (when pulled up)		–250	–30	–2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		-1	—	—		
Input current 3 (TEST)	IIH3	VIH3 = V_{DD}		20	300	1500		
	IIL3	VIL3 = V_{SS}		-1	—	—		

DC Characteristics (5 of 5)

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = AV_{SS} = SPV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

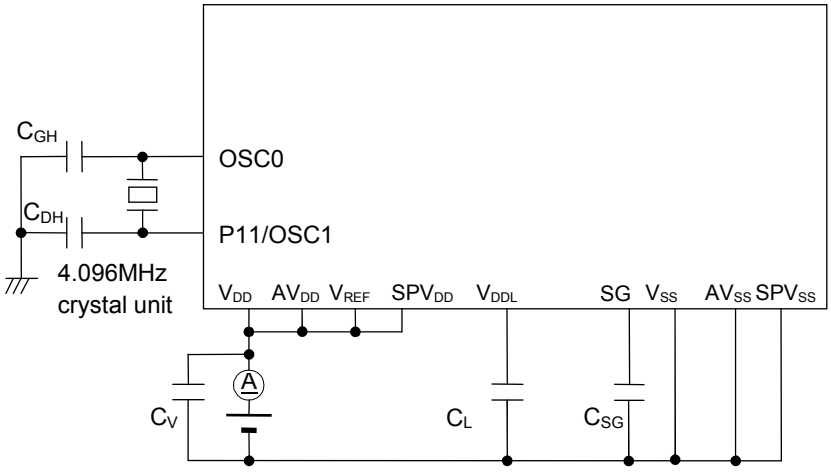
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P07) (P11) (P30–P37) (P40–P47)	VIH1	—	0.7× V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3× V_{DD}		
Hysteresis width (RESET_N) (TEST) (NMI) (P00–P07) (P11) (P30–P37) (P40–P47)	ΔVT	—	0.05× V_{DD}	—	0.4× V_{DD}		
Input pin capacitance (NMI) (P00–P07) (P11) (P30–P37) (P40–P47)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

Hysteresis Width



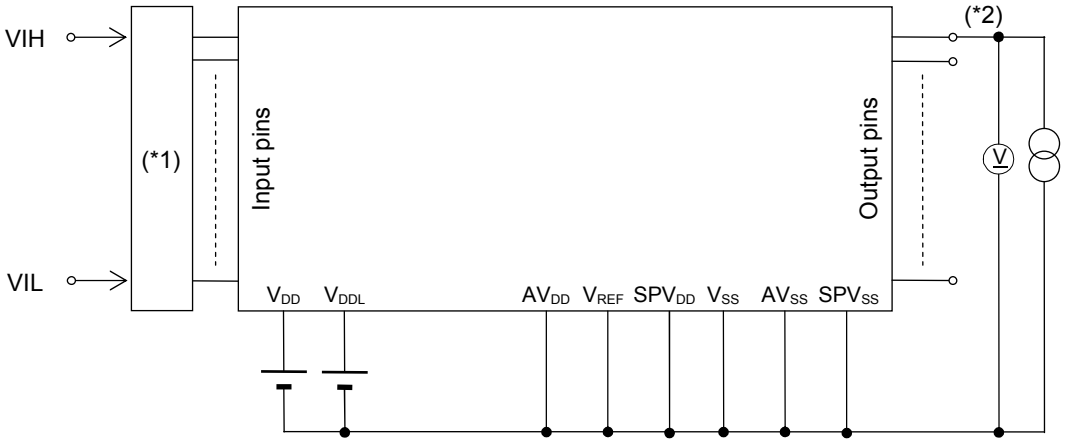
Measuring Circuits

Measuring circuit 1



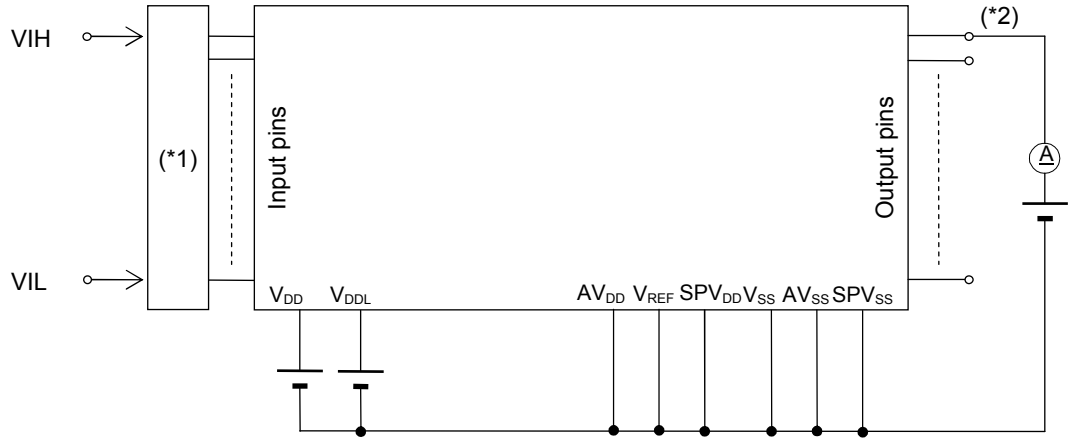
C_V : 1 µF
C_L : 10 µF
C_{SG} : 0.1 µF
C_{GH} : 24 pF
C_{DH} : 24 pF
4.096 MHz crystal unit:
HC49SFWB (Kyocera)

Measuring circuit 2



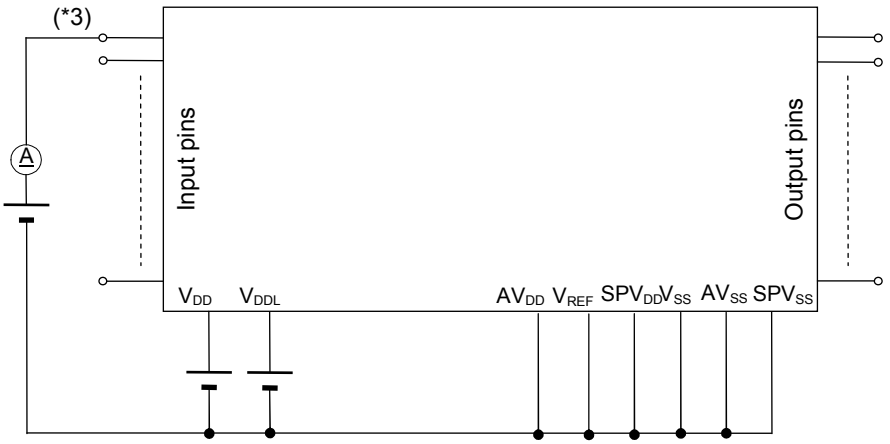
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 3



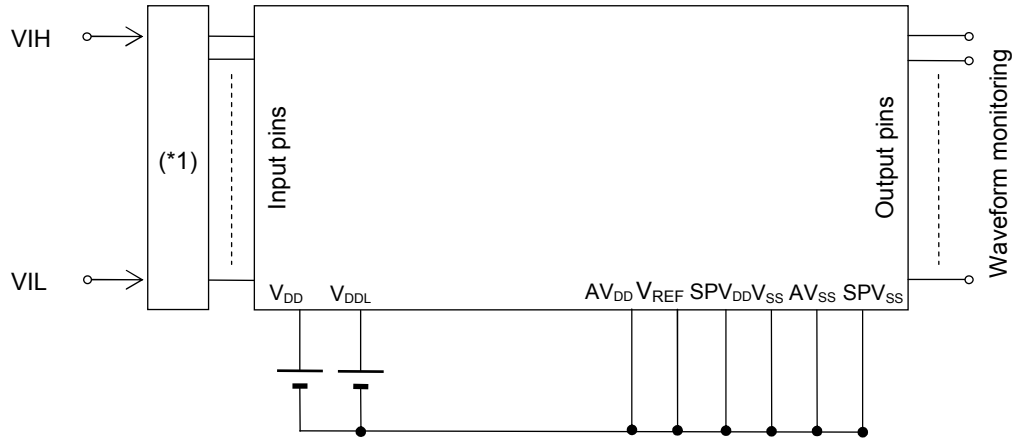
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 4



*3: Measured at the specified input pins.

Measuring circuit 5

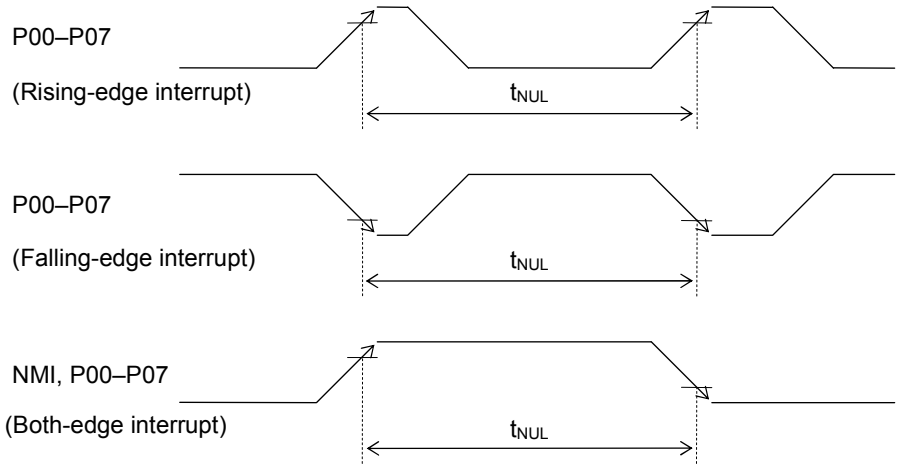


*1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = AV_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5× sysclk	—	3.5× sysclk	µs

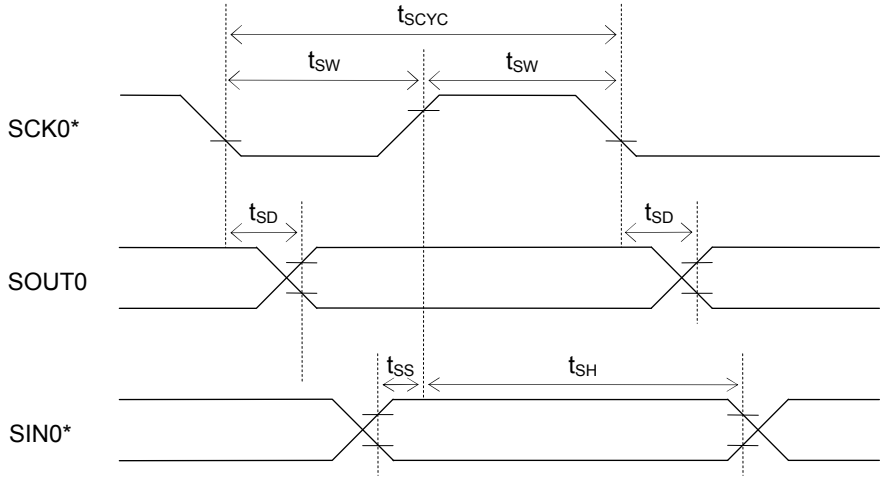


AC Characteristics (Synchronous Serial Port)

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = AV_{SS} = 0V, Ta = −40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	µs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	µs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected by S0CK3–0 of the serial port 0 mode register (SIO0MOD1)



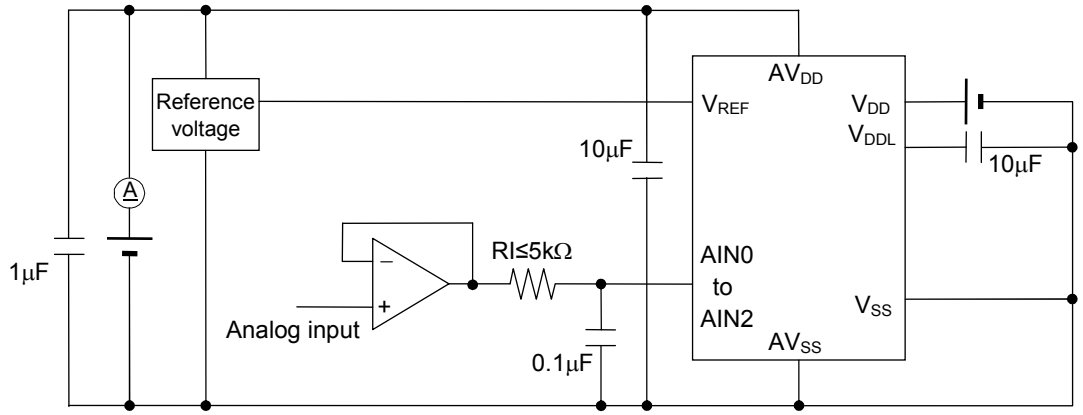
*: Indicates the secondary function of the corresponding port.

Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD} = SPV_{DD} = AV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

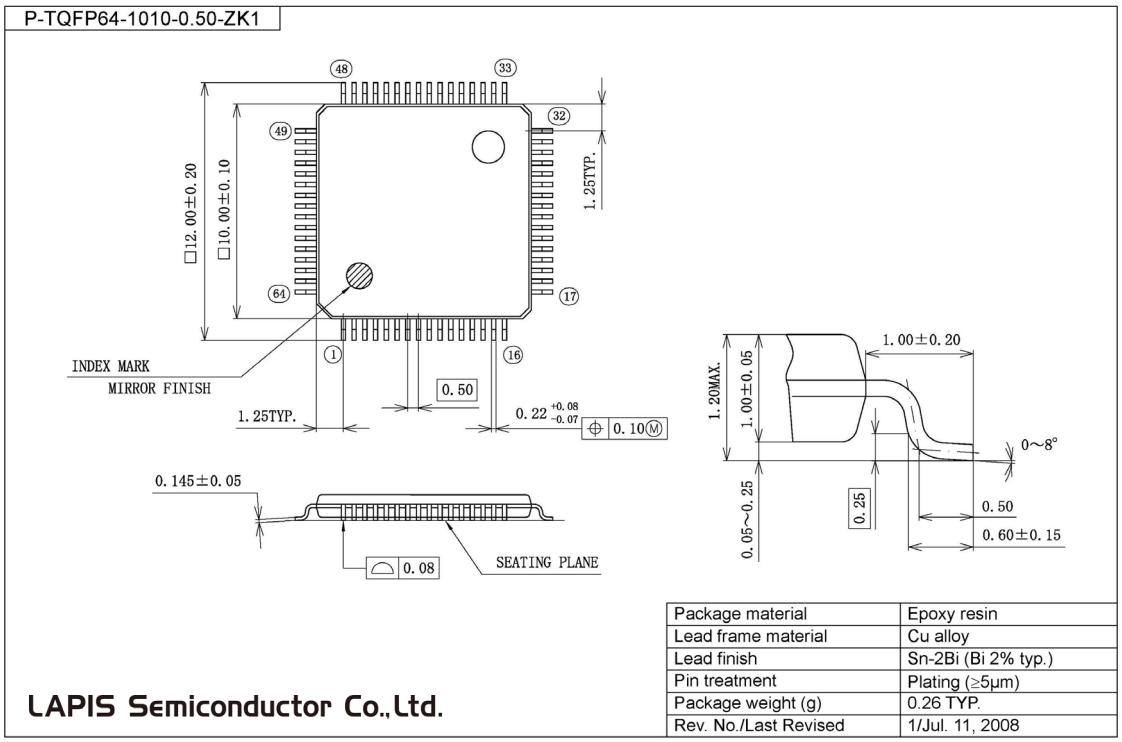
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	12	bits
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 5.5V	–4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 5.5V	–3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	SACK=0 (HSCLK=375kHz to 625MHz)	—	25	—	φ/CH
		SACK=1 (HSCLK=1.5MHz to 4.2MHz)	—	112	—	

φ: Period of high-speed clock (HSCLK)



PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Plating (≥5μm)
Package weight (g)	0.26 TYP.
Rev. No./Last Revised	1/Jul. 11, 2008

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	JEDEC (W/L/t=76.2/114.5/1.6(mm))
PCB Layer	4L
Air cooling conditions	Calm(0m/sec)
Heat resistance(θJa)	50[℃/W]
Power consumption of Chip PMax at OutputPower 1W (5V)	0.818[W]
Power consumption of Chip PMax at OutputPower 0.5W (3.3V)	0.283[W]

TjMax of this LSI is 125℃. TjMax is expressed with the following formulas.

TjMax = TaMax + θJa × PMax

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q346FULL-01	Jan 7, 2010	–	–	Formally edition 1

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